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10/661,593	09/15/2003	Shinichi Yasuda	242823US2RD	8075

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EXAMINER
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ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/661,593	YASUDA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10 and 22-30* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10 and 22-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/11/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 12/11/2008.

2. Claims 1-2, 4-8, 10 and 22-30 are pending in this application. Claims 1, 22 and 29-30 are independent claims. In Amendment, claims 3, 9 and 21 are cancelled; claims 29-30 are added; and claims 11-20 are withdrawn from consideration. This Office Action is made final.

Claim Objections

3. Claims 22 and 30 are objected to because of the following informalities:

Re claims 22 and 30, the applicant is requested to write out the term "CR" in full for clarification purposes,

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 29-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 29, the newly added limitation "a frequency of each occurrence of "0" and "1" becomes closer to 0.5" is mis-descriptive since number/frequency of each occurrence of bit can never be ½ due to the fact there is no ½ occurrence. For

examination purposes, the Examine considers the newly added limitations as the probability of each occurrence of "0" and "1" becomes closer to ½. Claim 30 has the same rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 7-8, 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chevalier (U.S. 3,866,029) in view of Tenemasa et al. ("Physical Random-Number Generator Using Schottky MOSFET").

Re claim 1, Chevalier discloses in Figure 1 a random number generator (e.g. output of Figure 1 and abstract as general concept of random number generator architecture), comprising: a counter circuit (e.g. binary counter 20 in Figure 1) configured to be supplied with a clock signal and a random signal (e.g. output of clock input 34 and random bits 11 respectively in Figure 1) and to provide a count value of the clock signal with respect to a transition of the random signal (e.g. output of component 20 as Ci in Figure 1); and a first latch circuit (e.g. component 21 in Figure 1 as latch component) configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal (e.g. output of component 30 as random number in Figure 1) and wherein when a frequency of the clock signal increases, a bias of a

frequency of occurrence of "0" and "1" becomes smaller (e.g. abstract wherein as more and more random bits come out of device, the chance or probability as bias of having 0 or 1 is almost the same as ½ due to randomness).

Chevalier fails to disclose the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which said random signal is supplied. However, Tenemasa et al. disclose in Figure 4 the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which said random signal is supplied (e.g. Figure 4 and paragraph right after section "3. Circuit and Operation" in page 96).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which said random signal is supplied as seen in Tenemasa et al.'s invention into Chevalier's invention because it would enable to simplify and compact the circuit for generating random number (e.g. section "1. Introduction" in page 96).

Re claim 2, Chevalier further discloses in Figure 1 the random signal manifests a characteristic in which power spectrum intensity varies with an increase of frequency (e.g. inherently property of random signal wherein as increasing frequency of random signal, the power spectrum intensity of the random signal must decrease respect to the

frequency of the random signal, and Figure 1 with component 11 as random bits generator adjustment).

Re claim 7, Chevalier further discloses in Figure 1 a pulse counter is accessible by the clock enable input, and the output of the pulse counter becomes the random signal (e.g. Figure 1 with clock input 34 and random bits 11).

Re claim 8, Chevalier further discloses in Figure 1 an inverter connected between the clock enable input side and a clock input side of the first latch circuit (e.g. load/enb signal in Figure 1).

Re claim 10, Chevalier fails to disclose in Figure 1 the first latch circuit is a D type flip-flop. However, D type flip-flop is well known and widely used in the technology of art as the examiner takes an Official notice.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the first latch circuit is a D type flip-flop into Chevalier's latch because it would enable to capture/output the signal at the moment the clock goes high.

Re claim 29, it has similar limitations cited in claim 1. Thus, the most of the limitations in claim 29 are also rejected under the same rationale as cited in the rejection of rejected claim 1. In addition, Chevalier further discloses the frequency of each occurrence of "0" and "1" becomes closer to 0.5 (e.g. abstract wherein as more and more random bits come out of device, the chance or probability as bias of having 0 or 1 is almost the same as ½ due to randomness).

8. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chevalier (U.S. 3,866,029) in view of Tenemasa et al. ("Physical Random-Number Generator Using Schottky MOSFET"), as applied to claim 1 above, and in further view of Kent (U.S. 5,222,142).

Re claim 4, Chevalier in view of Tenemasa et al. fail to disclose in Figure 1 a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal. However, Kent discloses in Figure 5 a second latch circuit (e.g. component 48/16 in Figure 5) configured to receive a random number acquisition clock signal having a constant period (e.g. clock signal) and the first random number signal (e.g. output of 46 in Figure 5), to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal (e.g. output of component 48/16 in Figure 5).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal as seen in Kent's Figure 5 into Chevalier in view of Tenemasa et al.'s invention because it would enable to improve the randomized number (e.g. col. 2 lines 37-52).

Re claim 5, Chevalier further discloses in Figure 1 the frequency of the random number acquisition clock is lower than the frequency of the random signal (e.g. Figure 1).

Re claim 6, Chevalier in view of Tenemasa et al. and in further view of Kent fail to disclose in Figure 1 the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level. However, the examiner takes an Official notice that the transition occurs at the raising level by clock signal is well known in the art of technology.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level into Chevalier in view of Tenemasa et al. and in further view of Kent's latch because it would enable to capture/output the signal at the moment the clock goes high.

9. Claims 22, 26-28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chevalier (U.S. 3,866,029) in view of Horowitz Paul ("The Art of Electronics").

Re claim 22, Chevalier discloses in Figure 1 a random number generator (e.g. output of Figure 1 and abstract as general concept of random number generator architecture), comprising: a counter circuit (e.g. binary counter 20 in Figure 1) configured to be supplied with a clock signal and a random signal (e.g. output of clock input 34 and random bits 11 respectively in Figure 1) and to provide a count value of the clock signal with respect to a transition of the random signal (e.g. output of component 20 as Ci in Figure 1); and a first latch circuit (e.g. component 21 in Figure 1 as latch component)

configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal (e.g. output of component 30 as random number in Figure 1), and wherein when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller (e.g. abstract wherein as more and more random bits come out of device, the chance or probability as bias of having 0 or 1 is almost the same as ½ due to randomness).

Chevalier fails to disclose explicitly in Figure 1 a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency, wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal. However, Horowitz Paul discloses in the article a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency (e.g. lines 11-21 right column in page 305), wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal (e.g. Figure 7.47 in page 305).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency, wherein the source comprises an oscillation circuit

using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal as seen in Horowitz Paul's invention into Chevalier's invention because it would enable to generating high frequency random number source (e.g. lines 11-21 right column in page 305 and Figure 7.47 in page 305).

Re claim 26, it has similar limitations cited in claim 7. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 27, it has similar limitations cited in claim 8. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 28, it has similar limitations cited in claim 10. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 30, it has similar limitations cited in claim 22. Thus, the most of the limitations in claim 30 are also rejected under the same rationale as cited in the rejection of rejected claim 22. In addition, Chevalier further discloses the frequency of each occurrence of "0" and "1" becomes closer to 0.5 (e.g. abstract wherein as more and more random bits come out of device, the chance or probability as bias of having 0 or 1 is almost the same as ½ due to randomness).

10. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chevalier (U.S. 3,866,029) in view of Horowitz Paul ("The Art of Electronics"), as applied to claim 22 above, and in further view of Kent (U.S. 5,222,142).

Re claim 23, Chevalier in view of Horowitz Paul fail to disclose in Figure 1 a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal. However, Kent discloses in Figure 5 a second latch circuit (e.g. component 48/16 in Figure 5) configured to receive a random number acquisition clock signal having a constant period (e.g. clock signal) and the first random number signal (e.g. output of 46 in Figure 5), to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal (e.g. output of component 48/16 in Figure 5).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal as seen in Kent's Figure 5 into Chevalier in view of Horowitz Paul's invention because it would enable to improve the randomized number (e.g. col. 2 lines 37-52).

Re claim 24, Chevalier further discloses in Figure 1 the frequency of the random number acquisition clock is lower than the frequency of the random signal (e.g. Figure 1).

Re claim 25, Chevalier in view of Horowitz Paul and in further view of Kent fail to disclose in Figure 1 the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the

random number acquisition clock signal changes from a low level to a high level. However, the examiner takes an Official notice that the transition occurs at the raising level by clock signal is well known in the art of technology.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level into Chevalier in view of Horowitz Paul and in further view of Kent's latch because it would enable to capture/output the signal at the moment the clock goes high.

Response to Arguments

11. Applicant's arguments filed 12/11/2008 have been fully considered but they are not persuasive.

a. The applicant repeatedly argues in pages 10-13 for claims rejected under 35 U.S.C. 103(a) that neither the cited references would disclose the newly added limitation "when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller. Further, the applicant alleges that no matter how the teaching of each references, the combination of references does not teach or suggest a random number generator in which when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller as cited in the claimed invention.

The examiner respectfully submits that the specific newly added limitation above is reasonably seen in Figure 1, abstract, and claim 1 of the primary reference by Chevalier alone wherein as the clock input 34 in Figure 1 is increased, the more random bits are generated by generator 11 and counter 20 which produce the random sequences wherein the probability of having 0 and having 1 in the random sequences is equal to ½ as seen in abstract and claim 1. If the probability or chance of having 0 or 1 at the random sequence output is ½, then mathematical inherently indicates or shows the offset of bias having 0 over 1 or having 1 over 0 is close 0 due to randomness of the sequence.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

February 11, 2009